Consumer Microcircuits Limited

PRODUCT INFORMATION

FX709 Voice Store Retrieve CVSD Codec

Publication D/709/6 July 1994

Features/Applications

- CVSD Encode + Decode
- Programmable Clock Rates
- Programmable Voice Filters
- Voice Power Output
- Voice Spectrum Monitor
- 8-bit Memory/Instruction I/O
- Processor Interface
- Voice Message Mailbox
- Status Annunciators
- Re-try Message Forward
- Voice Security Scrambling
- Voice Data Communications
- Time/Frequency Companding
- Audio Delay Functions

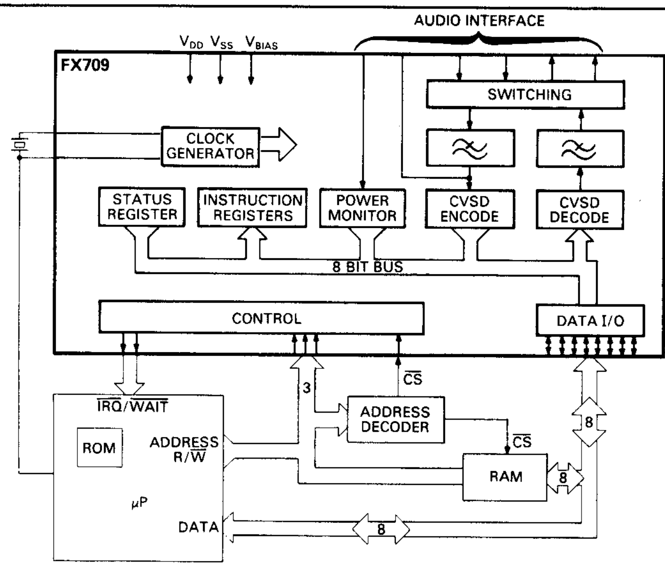


Fig. 1 System Schematic Diagram

FX709

Brief Description

The FX709 is an audio-digital interface codec for microprocessor controlled Voice Store and Retrieve applications.

In encode, audio input signals are band-limited by a lowpass filter and digitised by a CVSD 1-bit serial encoder. After conversion to 8-bit parallel format, encoded data is read to the I/O bus for storage in memory.

In decode, memory contents written into the I/O port are converted back to 1-bit serial form and decoded by a CVSD decoder. The decoder output is lowpass filtered and output as retrieved audio.

The audio encode/decode functions are independently controlled, permitting concurrent or asynchronous VSR operations to be performed. Time and frequency companding is available via independently programmable encode/decode data rates and filter cut-offs.

Support for VOX functions and 'Pause' memory management is provided by the power assessment register.

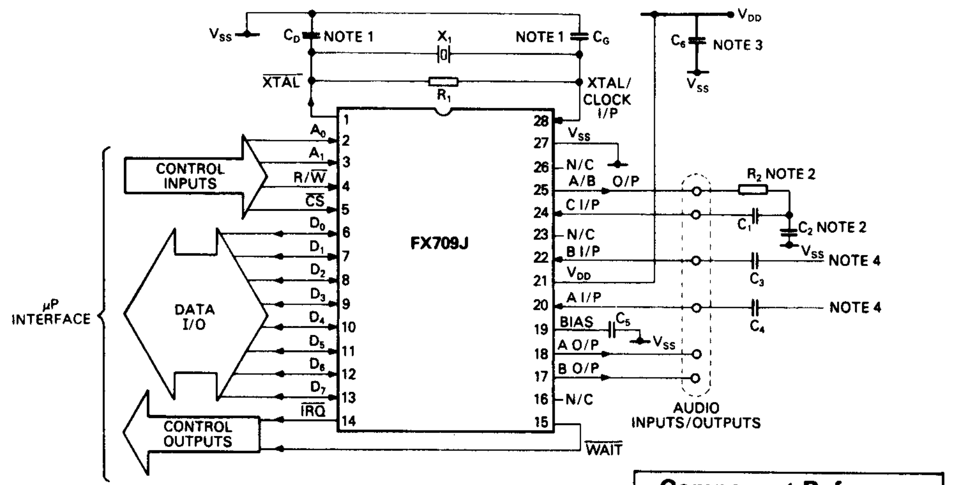
This contains two 4-bit numbers representing the average signal levels into the data encoder and a replica encoder over a programmable averaging period.

The device instruction set includes input/output signal switching and a standby powerdown function. The FX709 is a lowpower CMOS circuit and uses a single 5 volt supply.

Pin Number FX709J/LH	Function
1	**$\overline{\text{Xtal}}$:** Output of clock oscillator inverter.
2	**A_0:**
3	**A_1:** These pins determine which register may be addressed via the I/0 port.
4	**R/$\overline{\text{W}}$:**

A_0	A_1	R/$\overline{\text{W}}$	Register
0	0	0	'A' instruction
1	0	0	'B' instruction
0	1	0	Decoder
1	1	0	No Register
0	0	1	Status
1	0	1	Power
0	1	1	Encoder
1	1	1	No Register

Pin Number FX709J/LH	Function
5	**$\overline{\text{CS}}$:** Chip Select input, this input has a 1 MΩ pullup to V_{DD}.
6	**D_0:** I/0 Port
7	**D_1:** I/0 Port
8	**D_2:** I/0 Port
9	**D_3:** I/0 Port
10	**D_4:** I/0 Port
11	**D_5:** I/0 Port
12	**D_6:** I/0 Port
13	**D_7:** I/0 Port
14	**$\overline{\text{IRQ}}$:** Interrupt Request Output, this pin is the output of the interrupt request generator. This device can be "wire OR'd" with other active-low components. See section on Interrupt Requests. (100kΩ internal pullup to V_{DD}).
15	**$\overline{\text{WAIT}}$ Output:** The circuit requires a minimum Chip Select time of t_{ACS}. If the host µP has a CS time of less than this the WAIT output must be used to delay the µP when accessing the FX709. (See Figure 7). (100kΩ internal pullup to V_{DD}). *NOTE:* If the WAIT output is to be used, then to prevent spurious operation of this function during Power-Up, it is recommended that: a: Power-Up of the FX709 is delayed until µP Power-Up is complete, or, b: The Chip Select input is held open-circuit during the FX709 Power-Up sequence.
16	No connection.
17	**Analogue Output B:** (See Figure 4).
18	**Analogue Output A:** (See Figure 4).
19	**V_{BIAS}:** The bias or analogue ground pin and is internally set to $V_{DD}/2$. It should be decoupled to V_{SS} with a capacitor of 1.0µF (min.).
20	**Analogue Input A:** (See Figure 2, Note 4 and Figure 4).
21	**V_{DD}:** Positive Supply.
22	**Analogue Input B:** (See Figure 2, Note 4 and Figure 4).
23	No connection.
24	**Analogue Input C:** This is the analogue input to the power encoder.
25	**Analogue Output A/B:** (See Figure 4).
26	No connection.
27	**V_{SS}:** Negative supply.
28	**Xtal/Clock Input:** This is the input to the clock oscillator inverter. A 1.0 MHz Xtal input or externally derived clock is injected at this pin.



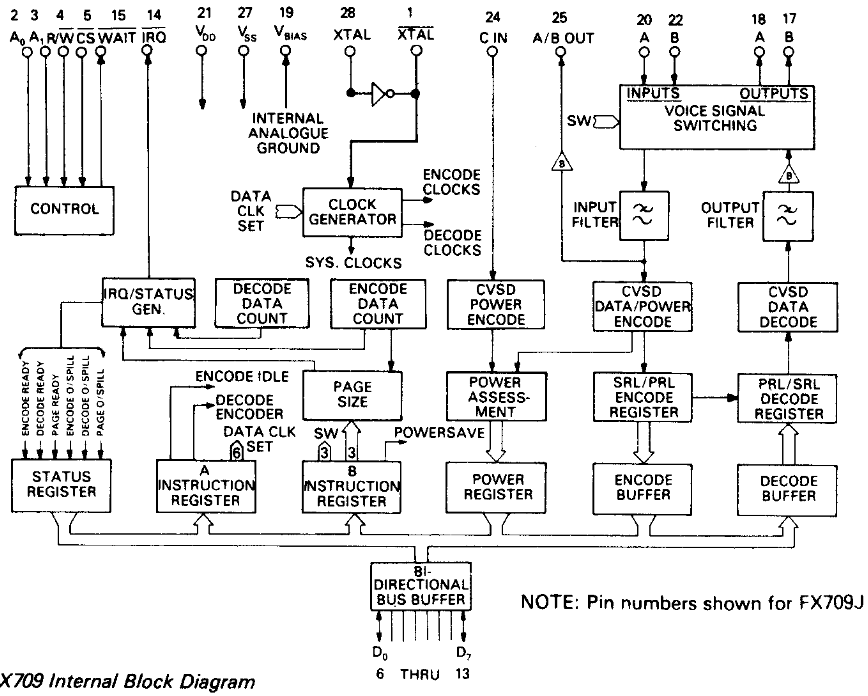
NOTES:

1. *C_G used to reduce voltage overshoot. Refer to CML Crystal application Applications Note D/XT/1 April 86.*
2. *R_2, C_2 forms a lowpass filter input to 'C' input power assessment circuit. The values shown represent a 820Hz lowpass although other cutoff frequencies may be selected depending on the application — see page 9.*
3. *Additional decoupling may be necessary for noisy supplies.*
4. *To prevent unwanted internal oscillations at the Encoder input pins, the source impedance to these inputs must be less than 100Ω. Output idle channel noise levels will improve with even lower source impedances.*

Component References

Component	Unit Value	Tolerance
R_1	>1M	±10%
R_2	5.6k	±10%
C_G	68p	Note 1
C_D	33p	Note 1
C_1	0.1µ	±20%
C_2	33n	±20%
C_3	0.1µ	±20%
C_4	0.1µ	±20%
C_5	1.0µ min	±20%
C_6	0.1µ	±20%

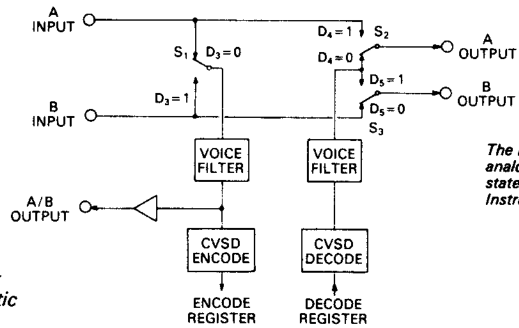
Fig. 2 External Component Connections



NOTE: Pin numbers shown for FX709J

Fig. 3 FX709 Internal Block Diagram

Analogue Switching



The input and output switching of analogue signals is controlled by the state of bit no's D_3, D_4 and D_5 in Instruction Register B.

Fig. 4 Audio Switching — Simplified Block Schematic

Frequency and Data Rate Control

Six bits of Instruction Register A (D_2 — D_7) control the data rates of the encoder and decoder and the bandwidths of the filters for the encoder and decoder. The configuration of the frequency dividers is as shown in the diagrams below and obtainable combinations of frequencies with various input clocks are listed.

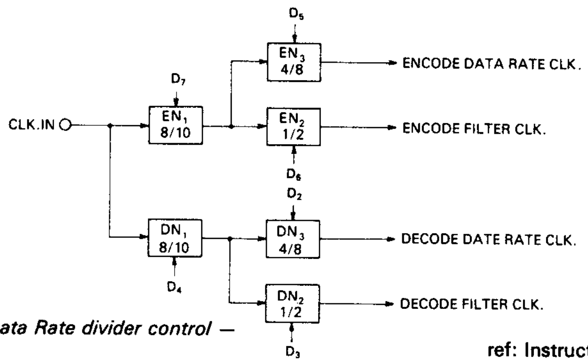


Fig. 5 Filter Clock and Data Rate divider control — Block diagram

ref: Instruction Register 'A'

CLOCK INPUT	N1	N2	FILTER CLOCK (Hz)	LOWPASS FILTER BW PB. ± 1dB	N3	DATA CLOCK (kbs)
2MHz	8	2	125k	3320	4	62.5
,,	8	2	125k	3320	8	31.25
,,	10	2	100k	2656	4	50.0
,,	10	2	100k	2656	8	25.0
1MHz	8	1	125k	3320	4	31.25
,,	8	1	125k	3320	8	15.625
,,	8	2	62.5k	1660	4	31.25*
,,	8	2	62.5k	1660	8	15.625*
,,	10	1	100k	2656	4	25.0
,,	10	1	100k	2656	8	12.5
,,	10	2	50k	1328	4	25.0*
,,	10	2	50k	1328	8	12.5*
2.048MHz	8	2	128k	3400	4	64.0
,,	8	2	128k	3400	8	32.0
,,	10	2	102.4k	2720	4	51.2
,,	10	2	102.4k	2720	8	25.6
1.024MHz	8	1	128k	3400	4	32.0
,,	8	1	128k	3400	8	16.0
,,	8	2	64k	1700	4	32.0*
,,	8	2	64k	1700	8	16.0*
,,	10	1	102.4k	2720	4	25.6
,,	10	1	102.4k	2720	8	12.6
,,	10	2	51.2k	1360	4	25.6*
,,	10	2	51.2k	1360	8	12.6*
614.4kHz	8	1	76.8k	2040	8	9.6*
768.0kHz	10	1	76.8k	2040	8	9.6*

***Caution**: Although possible, the Codec insertion loss is not according to the specification at these settings. (see Page 10).

Table 1 Possible combinations of clock input frequency, filter cutoff (Hz) and Data Clock (kbs)

Register Truth Tables

The following tables describe the function of each bit within each register. 'Address Input' logic states are shown in the top right hand corner of each table. The following registers are described below:

Instruction Register 'A'	[IRA]	pages 5 and 6
Instruction Register 'B'	[IRB]	pages 6 and 7
Status Register	[SR]	pages 8 and 9
Power Register	[PR]	page 9

IRA	INSTRUCTION REGISTER 'A'			A_0 = 0 A_1 = 0 $R/\overline{W}$ = 0
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_0	Encoder Idle	 1 0	SRD_3	D_0 sets the encoder idle/normal mode of operation. **FORCED**: Forces the encode register to fill with a 1010101... idle pattern. *Note: incoming encoded data is still available for the power assessment circuits.* **NORMAL**: Allows the encode register to fill with encoded data. Data is transferred to the encode buffer during the last bit of the encode byte.
D_1	Decoder Data Source In Overspill	 1 0	SRD_4	D_1 determines the source of data for the decoder. **ENCODER:** Internally connects the output of the encode register to the input of the decode register. This condition effectively connects the audio straight through. The encoded data may still be accessed via the encode buffer, and I/O port. Fills the decode register with idle pattern. In either case data may be loaded into the decode register via the I/O port. This automatically overwrites the current contents of the decode register.
D_2	Decode Data Rate Clock Divider	 1 0	Fig. 5 Table 1	D_2 sets the Decode data rate divider. ÷ 8 ÷ 4
D_3	Decode Filter Clock Divider	 1 0	Fig. 5 Table 1	D_3 sets the Decode Filter Clock Divider and hence the Filter Cut-off Frequency. ÷ 2 ÷ 1
D_4	Decode Master Clock Divider	 1 0	Fig. 5 Table 1	D_4 sets the Decode Master clock divider. ÷ 10 ÷ 8

IRA	INSTRUCTION REGISTER 'A'			A_0 = 0 A_1 = 0 $R/\overline{W}$ = 0
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_5	Encode Data Rate Divider	 1 0	Fig. 5 Table 1	D_5 sets the Encode Data Rate Divider. ÷ 8 ÷ 4
D_6	Encode Filter Clock Divider	 1 0	Fig. 5 Table 1	D_6 sets the Encode Filter Clock Divider and hence the filter cut-off frequency. ÷ 2 ÷ 1
D_7	Encode Master Clock Divider	 1 0	Fig. 5 Table 1	D_7 sets the Encode Master Clock Divider. ÷ 10 ÷ 8

IRB	INSTRUCTION REGISTER 'B'			A_0 = 1 A_1 = 0 $R/\overline{W}$ = 0
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_0 D_1 D_2	Page Size Set	See Notes		$D_0 - D_2$ set the "page size" in Encode Data bytes. (one byte = 8 serial data bits) in accordance with the table below: (see table below) Page Period (secs) = 8 x Page Bytes/Data Rate (b/s)
D_3	"A/B" Encode	 0 1	Fig. 4	D_3 defines which audio input A or B is connected to the encoder via the encode filter. (See fig. 4). **AUDIO INPUT "A"**: Internally connects the "A" audio input to the encode filter input. The "A/B OUT" pin outputs filtered audio "A". Audio input "B" set to $V_{DD}/2$. **AUDIO INPUT "B"**: Internally connects the "B" audio input to the encode filter input. The "A/B OUT" pin outputs filtered audio "B". Audio input "A" set to $V_{DD}/2$.

D_2	D_1	D_0	:	PAGE BYTES	Page Period @32kbs
0	0	0	:	32	8ms
0	0	1	:	64	16ms
0	1	0	:	96	24ms
0	1	1	:	128	32ms
1	0	0	:	160	40ms
1	0	1	:	192	48ms
1	1	0	:	224	56ms
1	1	1	:	256	64ms

IRB	INSTRUCTION REGISTER 'B'			A_0 = 1 A_1 = 0 $R/\overline{W}$ = 0
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_4	Switch Audio Output "A"	 1 0	Fig. 4	D_4 controls the Output Audio Switch to determine which source audio is connected to Audio Output "A" pin. Input "A" to Output "A" (direct). Decoder to Output "A".
D_5	Switch Audio Output "B"	 1 0	Fig. 4	D_5 controls the Output Audio Switch to determine which source audio is connected to Audio Output "B" pin. Decoder to Output "B" Input "B" to Output "B" (direct).
D_6	Powersave	 1 0		D_6 controls the enablement and disablement of all analogue circuit elements. **POWERSAVE MODE:** Disables the circuit elements, thereby effectively reducing current consumption. **OPERATING MODE:** All circuit elements enabled. **NOTE:** During POWERSAVE, inputs are biased $V_{DD}/2$. Outputs are biased $V_{DD}/2$ if IRB D_4/D_5 are set to "direct".
D_7	Power Sensitivity	 1 0		D_7 determines the sensitivity range of the power measuring circuits. **HIGH:** Low power input, assessment circuits have + 12dB gain over LOW Setting. **LOW:** Normal power assessment sensitivity range. **NOTE:** High input levels in the HIGH condition may lead to overflow, producing an ambiguous reading.

SR	STATUS REGISTER			$A_0 = 0$ $A_1 = 0$ $R/\overline{W} = 1$
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_0	Encode Data Ready			D_0 indicates that a byte of data has been encoded and can be read from the encode buffer.
		1		**READ BYTE:** Set high during the last bit of the byte shifted into the encode register. This condition causes an interrupt request.
		0		**NOT READY/OVERSPILL:** This condition occurs when: 1. The last data byte in the encode data register has been read. 2. Encode data overspill bit = 1 ie. $SRD_3 = 1$.
D_1	Decode Data Ready			D_1 indicates that a byte of data has been decoded and a new byte should be written to the decode buffer.
		1	SRD_4	**WRITE BYTE:** This condition occurs when the decode register has been loaded from its buffer, i.e. after the last bit of the previous byte has been clocked out of the register.
		0		**NOT READY/OVERSPILL:** This condition occurs when data has been written into the decode buffer or the decode data overspill condition is valid ($SRD_4 = 1$).
D_2	Page Ready			This bit indicates that a page of bytes has been encoded.
		1		**READ PAGE:** This condition occurs when the page counter has completed the last byte of a page. This is after power measurements have been written into PRD_0 to PRD_7 inclusive.
		0	SRD_5	**NOT READY/OVERSPILL:** This condition occurs when Power Register "PR" has been read or the page overspill condition is valid.
D_3	Encode Overspill	1		**OVERSPILL:** Indicates that the encode data was not read between two consecutive "encode data ready" flags. Encoded data bytes have been lost, and no further bytes will be transferred to the encode buffer.
		0		**NORMAL:** This condition occurs when data has been read from the encode buffer, following a data ready flag, $SRD_0 = 1$, or by writing to the decode buffer if both encode and decode overspill bits are set. (See 'Interrupts' page 9).
D_4	Decode Overspill	1		**OVERSPILL:** When this bit is set data transfer from the decode buffer to the decode register is inhibited. If the "DECODER/ENCODER BUS" ($IRAD_1$) is not set then the decode register will fill with idle pattern.
		0		**NORMAL:** This condition occurs when data has been written to the decode buffer following a data ready flag, $SRD_1 = 1$ or by reading the contents of the encode buffer if both encode and decode overspill bits are set. (See 'Interrupts' page 9).

SR	STATUS REGISTER			$A_0 = 0$ $A_1 = 0$ $R/\overline{W} = 1$
Bit	**Function Name**	**Logic State**	**References**	**NOTES**
D_5	Page Overspill	1		**OVERSPILL:** This state indicates that the power register was not read before the next page was completed.
		0		**NORMAL:** Power register "read" or IRB written.

PR	POWER REGISTER		$A_0 = 1$ $A_1 = 0$ $R/\overline{W} = 1$
Bit	**Function Name**	**Logic State**	**NOTES**
D_0 D_1 D_2 D_3	"A/B" Power LSB "A/B" Power MSB		$D_0 - D_3$ represent the average signal level of the last page of data in the range from +6dBm to −24dBm (at 1kHz) for the A or B input. The relationship between binary value and signal level is frequency dependant and exhibits pre-emphasis characteristics. (see fig. 9).
D_4 D_5 D_6 D_7	"C" Power LSB "C" Power MSB		$D_4 - D_7$ represent the average signal level of the last page of data in the range from +6dBm to −24dBm (at 1kHz) for the C input.

Interrupts

Three conditions can cause interrupt requests to the host microprocessor.

(i) The encode buffer contains an unread byte of data which is the most recent byte encoded.
(ii) The decode buffer is ready to receive the next consecutive byte for decoding.
(iii) The power register contains a power assessment for the most recent whole page encoded.

The status register indicates which of the above conditions are true.

If an interrupt condition remains unserviced and the condition becomes irrecoverably untrue, the status bit is cleared, the corresponding overspill bit is set and further interrupts are automatically inhibited. Also the encode and decode data buffers retain the data present when the data bit was set, i.e. register-buffer update is inhibited. The power register is updated at all times.

Condition (i) is serviced by a valid address to the encode buffer. Condition (ii) is serviced by a valid address to the decode buffer. If conditions (i) and (ii) have both become UNTRUE, servicing either buffer resets both to a cleared start position. Condition (iii) is serviced by reading the Power Register.

The C Input

By careful selection of the audio frequency filtering to the C input the A/B and C power words can be used in the processor to provide frequency as well as power information. This facility could be used for word, pause or voice recognition.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX709J	−30°C to + 85°C
	FX709LH	−30°C to + 70°C
Storage temperature range:	FX709J	−55°C to +125°C
	FX709LH	−40°C to + 85°C

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, Ø = f_{in} = 1kHz.

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply voltage		4.5	5.0	5.5	V
Supply Current		—	6	—	mA
Supply Current (Power Save)		—	1	—	mA
Supply Ripple		—	50	—	mV
Input Impedance (Audio)		100	—	—	kΩ
Output Impedance (Audio)		—	—	6	kΩ
Input Logic '1'		3.5	—	—	V
Input Logic '0'		—	—	1.5	V
Output Logic '1'	1	3.5	—	—	V
Output Logic '0'	1	—	—	1.5	V
Input Current (Logic I/P's)		—	—	1.0	μA
Input Capacitance (Logic I/P's)		—	—	7.5	pF
Output Logic '1' Source current	2	—	—	120	μA
Output Logic '0' Sink current	3	—	—	360	μA
Three State output leakage current		—	—	4	μA
Dynamic Characteristics					
Audio Input Level		—	500	—	mV (rms)
Insertion Loss, (direct)	4, 7	−1.5	—	+1.5	dB
Attenuation distortion *(See Fig. 6)*					
Clock bit Rate	5	8	—	64	k bits/s
Idle Channel Noise	4, 6	—	2.5	—	mV (rms)
Signal/Noise Ratio *(See Fig. 8)*					

Notes

1. *Load 50pF, 200kΩ.*
2. *V_{out} = 4.6V, not pins 14 ($\overline{IRQ}$) and 15 ($\overline{WAIT}$), these wire OR 'able pins have 100kΩ pullups .*
3. *V_{out} = 0.4V.*
4. *Measured from Codec audio input to audio output.*
5. *2.048MHz master clock ÷ 32.*
6. *32kHz clock.*
7. *For a load of > 100kΩ, (serial switch impedance is 3kΩ/switch, see Fig. 4.*

Typical Performance

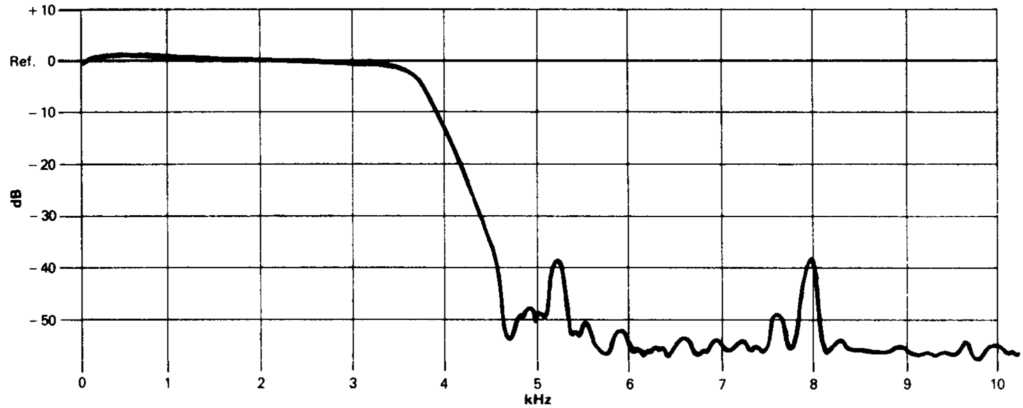
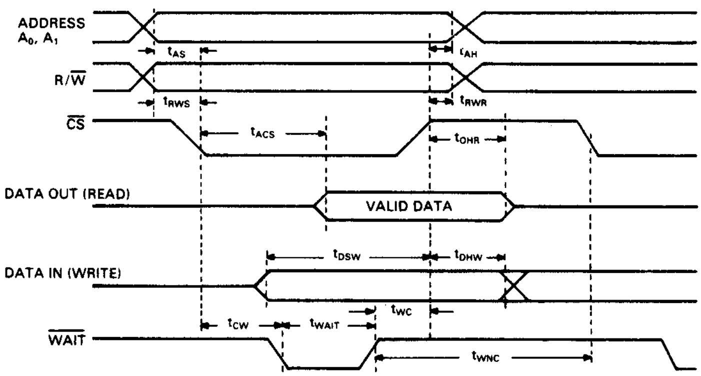


Fig. 6 Typical FX709 System Response measured at: filter 3320 Hz, V_{IN} –24 dBm, 32 kb/s



t=	Min.	Typ.	Max.	Units
t_{AS}	50	–	–	ns
t_{RWS}	50	–	–	ns
t_{AH}	0	–	–	ns
t_{RWR}	0	–	–	ns
t_{ACS}	–	–	250	ns
t_{OHR}	0	–	100	ns
t_{DSW}	150	–	–	ns
t_{DHW}	150	–	–	ns
t_{CW}	–	–	100	ns
t_{WAIT}	2	–	3	Xtal Cycle
t_{WC}	0	–	–	ns
t_{WNC}	2	–	–	Xtal Cycle

KEY

t_{AS} – Address Set Up Time
t_{RWS} – Read/Write Set Up Time
t_{AH} – Address Hold Time
t_{RWR} – Read/Write Recovery Time
t_{ACS} – Chip Select Access Time
t_{OHR} – Output Hold Time (Read)
t_{DSW} – Data Set Up Time (Write)
t_{DHW} – Data Hold Time (Write)
t_{CW} – Chip Select to WAIT Output
t_{WAIT} – WAIT Time
t_{WC} – WAIT High to Chip Select High
t_{WNC} – End of Wait to Next Chip Select

Fig. 7 Timing Diagram

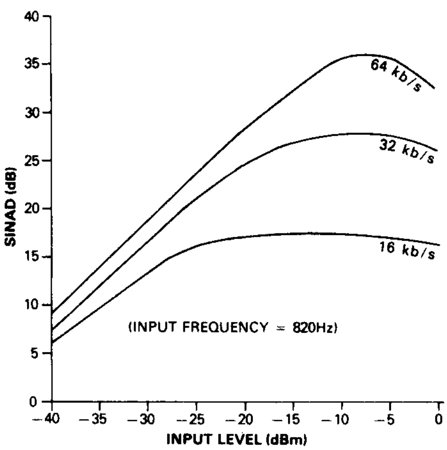


Fig. 8 Typical FX709 Sinad versus Input Level

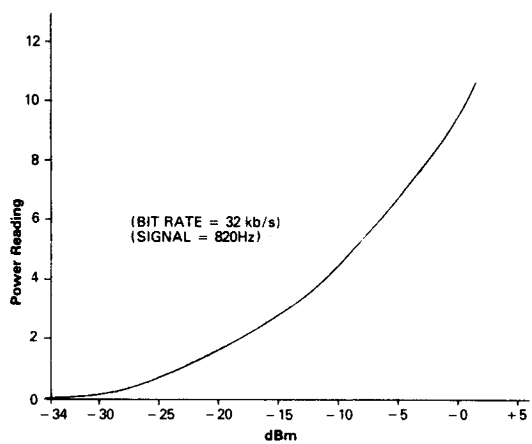


Fig. 9 Power Reading versus Input Level

Package Outlines

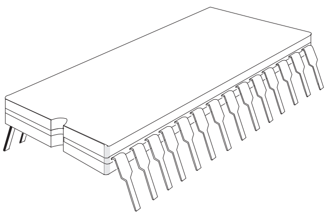
The FX709 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX709 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX709J 28-pin cerdip DIL (J5)

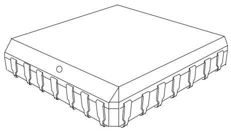
NOT TO SCALE



Max. Body Length 37.08mm
Max. Body Width 13.36mm

FX709LH 28-lead plastic leaded chip carrier (L3)

NOT TO SCALE



Max. Body Length 11.58mm
Max. Body Width 11.58mm

Ordering Information

FX709J 28-pin cerdip DIL (J5)

FX709LH 28-lead plastic leaded chip carrier (L3)